

IN THE CLAIMS

Please amend the claims as follows:

1. (Previously amended) An apparatus, comprising:
- a first memory cell coupled to a first bit line and a second bit line;
 - a second memory cell coupled to a third bit line and a fourth bit line;
 - an address decoder coupled to the first and second memory cells to enable access to the first and second memory cells;
 - a first comparator circuit coupled to the first and third bit lines to compare a voltage level on the first bit line with a voltage level on the third bit line at a time when data is output from the first memory cell on the first bit line and from the second memory cell on the third bit line; and
 - a second comparator circuit coupled to the second and fourth bit lines to compare a voltage level on the second bit line with a voltage level on the fourth bit line at a time when the compliment of the data that is output on the first and third bit lines is output from the first memory cell on the second bit line and from the second memory cell on the fourth bit line.
2. (Original) The apparatus of claim 1, wherein the address decoder decodes part of a memory address.
3. (Original) The apparatus of claim 1, wherein the first and second memory cells are dynamic RAM memory cells.
4. (Original) The apparatus of claim 1, wherein the first and second memory cells are static RAM memory cells.

5. (Previously amended) The apparatus of claim 1, wherein the first comparator circuit is comprised of a single comparator with a first input coupled to the first bit line and a second input coupled to the third bit line, and wherein the second comparator circuit is comprised of a single comparator with a first input coupled to the second bit line and a second input coupled to the fourth bit line.

6. (Previously amended) The apparatus of claim 5, wherein the output of the first comparator is coupled to a first latch to store an indication that the voltage level on the first bit line differs substantially from the voltage level on the third bit line, and wherein the output of the second comparator is coupled to a second latch to store an indication that the voltage level on the second bit line differs substantially from the voltage level on the fourth bit line.

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7. (Previously amended) The apparatus of claim 6, wherein the time at which the first and second latches are triggered is adjustable.

8. (Previously amended) The apparatus of claim 6, wherein the first latch is a sticky latch that is triggered to latch an indication that the voltage level on the first bit line differs substantially from the voltage level on the third bit line, and wherein the second latch is a sticky latch that is triggered to latch an indication that the voltage on the third bit line differs substantially from the voltage on the fourth bit line.

9. (Previously amended) The apparatus of claim 1, wherein the first and second comparator circuits are each comprised of:

a subtracting circuit with a first input coupled to the first bit line and a second input coupled to the second bit line;

a first comparator coupled to the output of the subtracting circuit; and

a second comparator coupled to the output of the subtracting circuit.

10. (Original) The apparatus of claim 9, wherein:

the output of the first comparator is coupled to a first latch to store an indication that difference in voltage levels between the first bit line and the second bit line has risen above a first reference voltage; and

the output of the second comparator is coupled to a second latch to store an indication that the difference in voltage levels between the first bit line and the second bit line has dropped below a second reference voltage.

11. (Original) The apparatus of claim 10, wherein the first and second reference voltages are adjustable.

12. (Original) The apparatus of claim 10, wherein the time at which the first and second latches are triggered is adjustable.

13. (Original) The apparatus of claim 10, wherein the first and second latches are sticky latches such that the first latch will latch any indication that the differences in voltage level between the first and second bit lines has risen above the first voltage reference and the second latch will latch any indication that the differences in voltage level between the first and second bit lines has dropped below the second reference voltage.

14. (Previously amended) A method, comprising:
writing identical values to the first and second memory cells;
coupling a first memory cell to a first bit line;
coupling the first memory cell to a second bit line;
coupling a second memory cell to a third bit line;
coupling the second memory cell to a fourth bit line;
coupling the first and third bit lines to inputs of a first comparator circuit;
coupling the second and fourth bit lines to inputs of a second comparator circuit;
reading the identical values from the first memory cell through the first bit line and from the second memory cell through the third bit line;
reading the identical values from the first memory cell through the second bit line and from the second memory cell through the fourth bit line that are compliments of the values read through the first and third bit lines;
comparing the voltage levels on the first and third bit lines; and
comparing the voltage levels on the second and fourth bit lines.

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15. (Previously amended) The method of claim 14, further comprising latching an indication from the first comparator circuit of whether or not the voltage level of the first bit line differs substantially from the voltage level of the third bit line, and latching an indication from the second comparator circuit of whether or not the voltage level of the second bit line differs substantially from the voltage level of the fourth bit line.

16. (Previously amended) The method of claim 14, further comprising setting the degree to which the difference in voltage levels between

the first bit line and the third bit line, and between the second bit line and the fourth bit line are substantial.

17. (Cancelled) A comparator circuit in a memory array comprising:
a first input coupled to a first bit line that is coupled to a first memory cell in the memory array;

a second input coupled to a second bit line that is coupled to a second memory cell in the memory array; and

an output coupled to a sticky latch.

18. (Cancelled) The comparator circuit of claim 17, wherein the comparator circuit is coupled to a multiplexer to disconnect the second bit line, and to connect a third bit line that is coupled the first memory cell in the memory array.

19. (New) An apparatus comprising:

a first bit line coupled to a first memory cell in a memory array;

a second bit line coupled to a second memory cell in the memory array;

a third bit line coupled to the first memory cell in the memory array;

a multiplexer coupled to both the second and third bit lines; and

a comparator having a first input coupled to the first bit line, and a second input coupled to the multiplexer to be selectively coupled to either the second or third bit line as selected by the multiplexer.

20. (New) The apparatus of claim 19, wherein the first and second memory cells are dynamic RAM memory cells.

21. (New) The apparatus of claim 19, wherein the first and second memory cells are static RAM memory cells.

22. (New) The apparatus of claim 19, wherein the output of the comparator is coupled to a latch to store an indication that the voltage level on the first bit line differs substantially from the voltage level on the third bit line.

23. (New) The apparatus of claim 22, wherein the time at which the latch is triggered is adjustable.

24. (New) The apparatus of claim 22, wherein the latch is a sticky latch that is triggered to latch an indication that the voltage level on the first bit line differs substantially from the voltage level on the third bit line.